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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/736,486	12/15/2003	Daniel Wang	669-77 CON/CIP	3800

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EXAMINER	
WARREN, MATTHEW E	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 06/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/736,486	WANG, DANIEL	
	Examiner	Art Unit	
	Matthew E. Warren	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the Amendment filed on March 28, 2005.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-5, 8-10, 12-17, 23, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ichitani et al. (US 6,120,301) in view of Kimura (US 5,396,104).

In re claims 1, 8, 13, and 23, Ichitani et al. discloses (col. 7, line 52 –col. 8, line 19 and figs. 1a and 1b) a method of packaging a high-density integrated circuit with at least one microchip (22) disposed on a substrate and the integrated circuit package itself comprising; providing bond wires (23), forming an array or plurality of coated bonding pads (square portions connected to bond wires 23) in rows and columns on said microchip (there are two columns along the left and right edge and two rows along the top and bottom edge-the second row is not shown), and directly connecting any of the terminal pads to any of the coated bonding pads by attaching said bond wires between any of the bonding pads and any of the terminal pads (12). The substrate has at least one row of terminal pads arranged along a perimeter of the substrate, wherein the substrate has vias (14) connecting the terminal pads directly to connectors (13, 27) on an opposite side of the substrate. The substrate is sized and shaped to contain a

sufficient number of rows of terminal pads and associated vias so that horizontal traces are not required. The semiconductor chip (22) is mounted on a surface of the substrate inside the perimeter. Ichitani shows all of the elements of the claims except providing and attaching pre-insulated bond wires. Kimura discloses a method of forming a semiconductor package including providing pre-insulated bond wires. The method of forming the pre-insulated wires produce high quality insulated wires with a thin insulating coating and having a uniform thickness (col. 6, lines 39-44). The pre-insulated wires used in the semiconductors have excellent insulating and bonding properties making the semiconductors using the wires highly reliable and easily manufactured (col. 13, lines 42-53). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the bonding process of Ichitani by using pre-insulated bond wires as taught by Kimura to produce reliable semiconductor devices that are easy to manufacture.

In re claims 2-5, and 12, Ichitani shows (fig. 1a) that the bond pads are disposed at selected locations on the chip, and discloses that the bond pads and wires comprise metal. Although Ichitani does not disclose what metal is used, aluminum, gold, and copper are known materials used for bonding pads and wires. Kimura discloses (col. 3, lines 60-67) that gold or other metal is used for the insulated bond wires. Kimura also shows (fig. 3) that wires may be attached to bond pads by a ball shaped joint (2a).

In re claims 9, 10, Ichitani shows (fig. 1b) the method of packaging the circuit including coating the circuit with a protective encapsulating material (25) and providing the bonding pads at select locations over the entire surface of the microchip.

In re claims 14-17, and 25, Ichitani shows (fig. 1a-1b) that the substrate (11) is configured to contain a minimal number of layers that inherently reduce inductance, crosstalk, capacitance, etc. because it has the same structure and materials as the instant invention. The substrate is a single layer substrate and contains no lead frames. The opposite side of the substrate contains a ball grid array (13, 27) and each of the terminal pads connects to the balls of the grid array through vias (14) directly traversing the substrate.

Claims 6, 7, and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ichitani et al. (US 6,120,301) in view of Kimura (US 5,396,104) as applied to claims 1 and 8 above, and further in view of Ball (US Pub 2002/0045290 A1).

In re claims 6, 7, and 11, Ichitani in view of Kimura shows all of the elements of the claims except the plurality of microchips disposed on the substrate and being connected by the bond wires which Ball shows (fig. 4) to increase integrated circuit density. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the microchip of Ichitani and Kimura by forming a package having a plurality of microchips connected by bond wires on a substrate as taught by Ball to increase the integrated circuit density.

Claims 18-20 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ichitani et al. (US 6,120,301) in view of Kimura (US 5,396,104) as applied to claims 13 and 23 above, and further in view of Bockelman et al. (US 5,471,010).

In re claims 18-20 and 24, Ichitani et al. in view of Kimura shows all of the elements of the claims except the bond wires extending between the bond pads and terminal pads and being positioned to reduce parallelism between adjacent wires. Bockelman et al. shows (figs. 3-5) that insulated bond wires are positioned in a cross-over or twisted arrangement to reduce crosstalk in a circuit (col. 3, lines 12-33). The bond wires are attached in an X in line pattern as seen in fig. 3. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the wire pattern of Ichitani in view of Kimura by crossing the wires in an X pattern as taught by Bockelman to reduce crosstalk in the device.

Claims 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ichitani et al. (US 6,120,301) in view of Kimura (US 5,396,104) as applied to claims 13 above, and further in view of Murdoch (US 4,002,282).

In re claims 21 and 22, Ichitani et al. in view of Kimura shows all of the elements of the claims except the bond pad located in an interior portion of a surface of a chip. Although it is well known in the art to form bond pads in any desired configuration or pattern including a pad formed in the center of a chip, Murdoch shows (fig. 1) a method of attaching an insulated bond wire to a bond pad located in an interior portion of the surface of the chip. None of the references specifically disclose that the bond pad is electrically connected to a power or ground connection but it is well known in the art that bond would provide one of a power, ground, or I/O signal connection. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was

made to modify the bond pad configuration of Ichitani and Kimura by forming a bond pad in the interior of the chip because Murdoch teaches that it is well known in the art to form a bond pad pattern in such a desired configuration.

Response to Arguments

Applicant's arguments filed with respect to claims 1-25 have been fully considered but they are not persuasive. The applicant primarily asserts that the prior art references do not show all of the elements of the claims, specifically that Ichitani and Kimura fails to disclose the feature of directly electrically connecting any of the terminal pads to any of the coated bonding pads with the pre-insulated bond wires. The examiner believes that the cited art shows all of the elements of the claims. The applicant assumes that the bond wires of Ichitani cannot be connected to any of the specific pads of the chip because the wires are not insulated, but Ichitani does not specifically disclose anywhere that the bond wires have to be arranged in a specific configuration. Kimura discloses (col. 13, line 53-col. 14, line 5) that the coated bonding wires could be used for semiconductor devices without being shorted out by adjacent wires or other conductors. When the insulated wires of Kimura are combined with the device of Ichitani, the wires may be electrically connected to any of the terminal pads and bond pads. As stated in the rejection above, Ichitani shows that there are a plurality of rows and columns. As seen in figure 1(a), there or two vertical columns of bond pads on the edges of the chip (22) and at least one row of bond pads on the upper peripheral edge of the chip (22). The other row of bond pads is not shown due to the

cut-away portion below. Therefore, Ichitani shows the plurality of rows and columns over the surface of the chip as recited in independent claim 8. The applicant further attacks the combination of Ichitani and Kimura by stating that it is not necessary to protect the bonding wires of Ichitani due to the specific configuration of bonds. However, Ichitani may still benefit from the wires being individually insulated and protected during the encapsulating process. When semiconductors are packaged with resin, the flow of the resin may sometimes move the wires and cause them to touch each other. By insulating the wires, one of ordinary skill in the art insures that wires are not touching each other and set in that manner during the encapsulation process.

The applicant further argues that Ichitani does not show that substrate is sized and shaped to provide a number of rows of terminal pads and associated via holes so that horizontal traces are not required because the substrate is multilayered. However, a representation of the package in figure 1(a) shows that the substrate may be a single layered design having the vias (14) formed directly under the terminal pads. There are no horizontal traces pictured and the terminal pads are connected to the solder terminals directly below with the vias (14). Thus, Ichitani discloses that limitation as well. In essence, the prior art references show all of the elements of the claims and this action is made final.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew E. Warren whose telephone number is (571) 272-1737. The examiner can normally be reached on Mon-Thur and alternating Fri 9:00-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MEW

June 15, 2005

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER